Amendments to the Claims:

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Canceled)

2. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the test unit ~~(120)~~ comprises a Read Only Memory (ROM).

3. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the test unit ~~(120)~~ comprises a read/write register.

4. (Currently amended) An electronic circuit ~~(402)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the test unit ~~(406)~~ comprises a combinatorial circuit ~~(502)~~ implementing an XNOR function and being connected to the I/O nodes.

5. (Currently amended) An electronic circuit ~~(402)~~ as ~~claimed in Claim~~ recited in claim 4, wherein a first selection ~~(410)~~ of the I/O nodes are arranged to carry respective input signals and a second selection ~~(412)~~ of the I/O nodes are arranged to carry respective output signals and wherein the test unit ~~(406)~~ is arranged according to the following rules:

each output signal results from an XNOR function having at least two input signals,

each output signal is dependent on a unique subset of the input signals,

each input signal contributes to at least one output signal via a particular XNOR function.

6. (Currently amended) An electronic circuit ~~(402)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the test unit ~~(406)~~ comprises a combinatorial circuit ~~(602)~~ implementing an XOR function and connected to the I/O nodes.

7. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the main unit ~~(110)~~ is arranged to bring the electronic circuit ~~(100)~~ into the test mode on receipt via a subset of the I/O nodes ~~(130)~~ of a predefined pattern or sequence of patterns.

8. (Currently amended) An electronic circuit ~~(100)~~ as ~~claimed in Claim 1~~ recited in claim 10, wherein the electronic circuit is provided with a test control node and wherein the electronic circuit is arranged to switch into the test mode on the basis of a signal value on the test control node.

9. (Currently amended) An electronic circuit as ~~claimed in Claim 1~~ recited in claim 10, wherein the main unit is a Synchronous Dynamic Random Access Memory

(SDRAM) and the test mode is activatable by a read action following power up of the electronic circuit.

10. (Currently amended) An electronic circuit ~~(100)~~ comprising:

a plurality of input/output (I/O) nodes ~~(130)~~ for connecting the electronic circuit to a further electronic circuit via interconnects,

a main unit ~~(110)~~ for implementing a normal mode function of the electronic circuit,

and a test unit ~~(120)~~ for testing the interconnects,

the electronic circuit having a normal mode in which the I/O nodes ~~(130)~~ are logically connected to the main unit ~~(110)~~ and a test mode in which the I/O nodes ~~(130)~~ are logically connected to the test unit ~~(120)~~,

~~characterised in that~~ wherein the test unit comprises at least one combinatorial circuit ~~(502)~~ implementing at least one of an XNOR function and an XOR function with at least two function inputs and a function output, the function inputs being connected to particular I/O nodes arranged to operate as input nodes of the test circuit and the function output being connected to a particular I/O node arranged to operate as output node of the test circuit.

11-13 (Canceled)